20V Dual N-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The XP8810 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-lin power loss are needed in a very small outline surface mount package

■ *FEATURE*

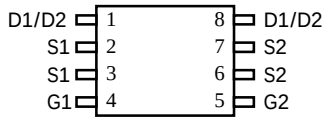
- ***20V/7A, $R_{DS(ON)}$=14mΩ (typ.)@VGS=4.5V***
- ***20V/5.5A, $R_{DS(ON)}$=18mΩ (typ.)@VGS=2.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- This is a Full RoHS compliance
- TSSOP8 package design
- ESD Rating:2000V HBM

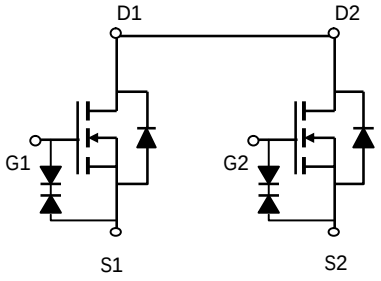
■ *APPLICATIONS*

- Power Management in Note Book
- Portable Equipment
- Battery Powered System

■ *PIN CONFIGURATION*

TSSOP-8
Top View





■ *PART NUMBER INFORMATION*

XP 8810AA-BB C	A=Package Code T: TSSOP8 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
XP8810 AT-TRG	T	TSSOP8	3000EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [A]	T_A=25°C	I_D	7	A
	T_A=70°C		6	
Pulsed Drain Current [B]		I_{DM}	30	
Power Dissipation [A]	T_A=25°C	P_D	1.5	W
	T_A=70°C		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ THERMAL DATA

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	64	83	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		89	120	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	53	70	°C/W

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

■ *ELECTRICAL CHARACTERISTICS(VDD=2.75V, T_A=25℃ Unless otherwise noted)*

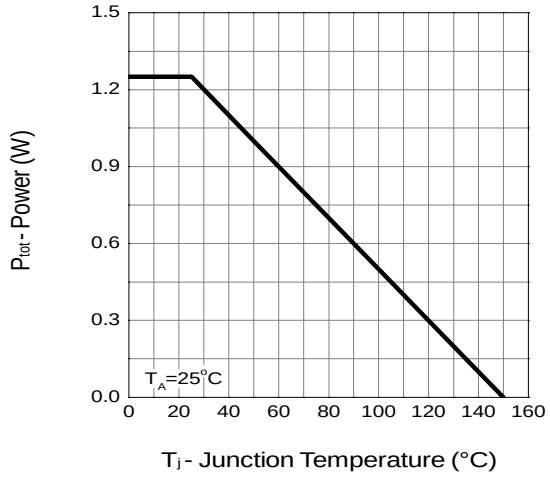
Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±4.5V			±1	μA
		V_{DS}=0V, V_{GS}=±8V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	0.4	0.6	1	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=7A	10	14.0	19	mΩ
		T_J=125°C	16	20	25	
		V_{GS}=4.0V, I_D=7A	11	15.5	19	mΩ
		V_{GS}=3.1V, I_D=6.5A	12	16	20	mΩ
		V_{GS}=2.5V, I_D=5.5A	13	18	22	mΩ
		V_{GS}=1.8V, I_D=5A	14	20	28	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=7A		31		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1.3	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		1120		pF
C_{oss}	Output Capacitance			195		pF
C_{rss}	Reverse Transfer Capacitance			155		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		4.0		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=7A		16		nC
Q_{gs}	Gate Source Charge			1.7		nC
Q_{gd}	Gate Drain Charge			6.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=5V, V_{DS}=10V, R_L=1.35Ω, R_{GEN}=3Ω		7.2		ns
t_r	Turn-On Rise Time			11		ns
$t_{D(off)}$	Turn-Off DelayTime			64		ns
t_f	Turn-Off Fall Time			32		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=7A, dI/dt=100A/μs		32		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7A, dI/dt=100A/μs		12		nC

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

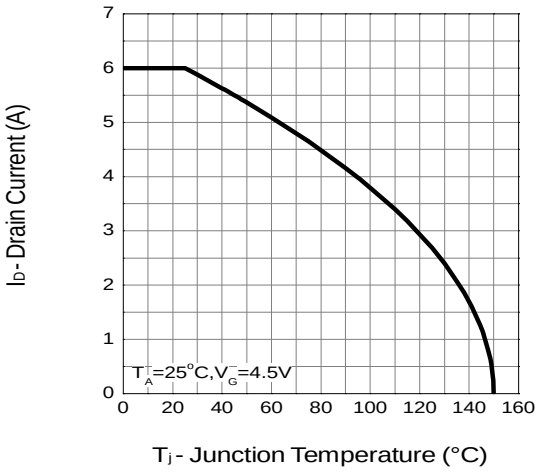
2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

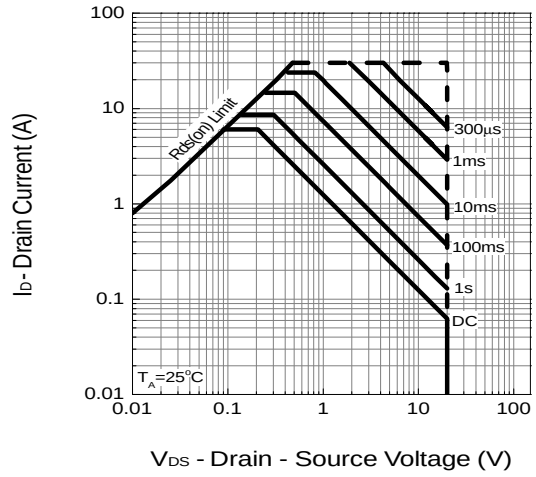
Power Dissipation



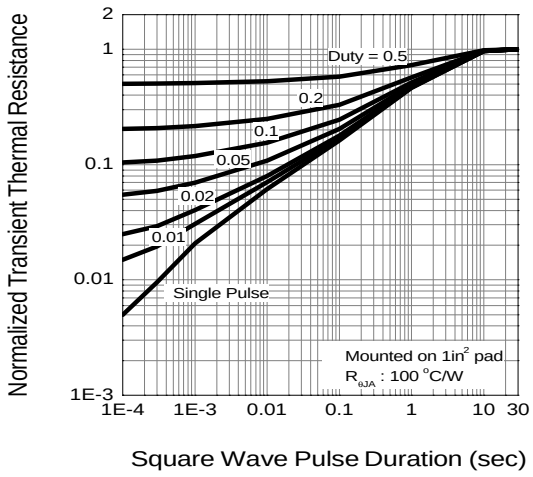
Drain Current



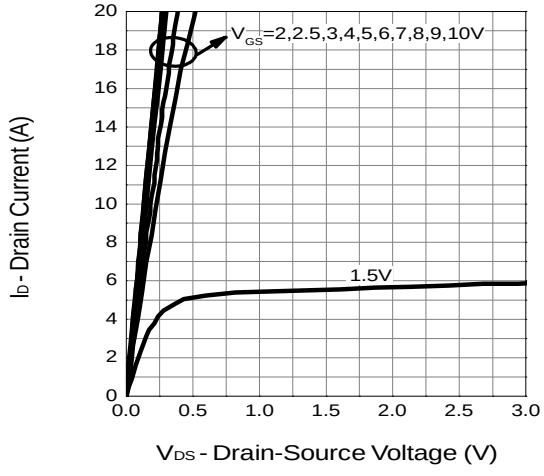
Safe Operation Area



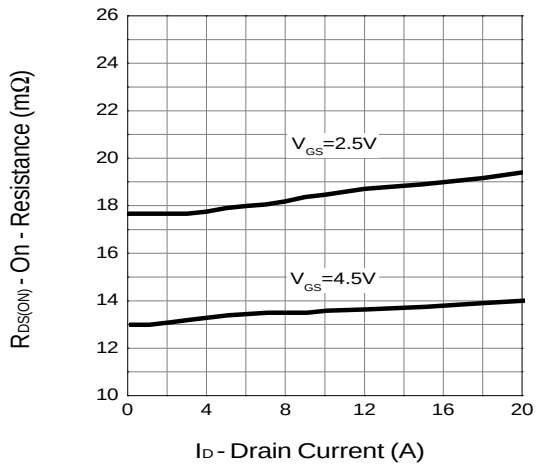
Thermal Transient Impedance



Output Characteristics

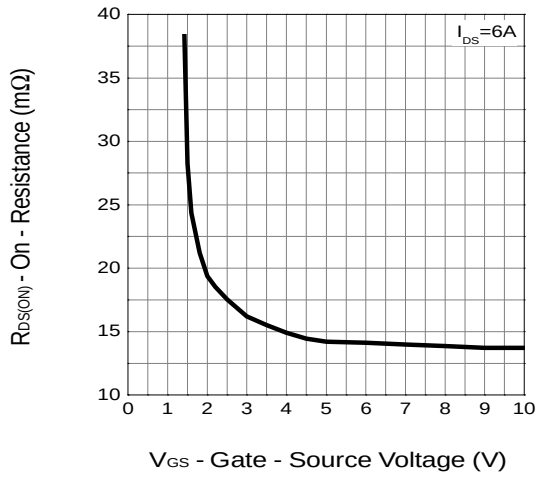


Drain-Source On Resistance



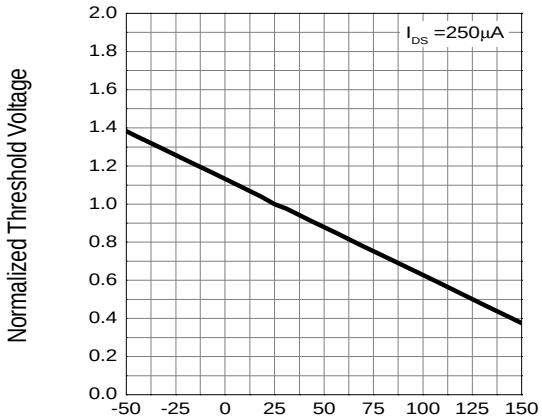
■ *TYPICAL CHARACTERISTICS (continuous)*

Gate-Source On Resistance



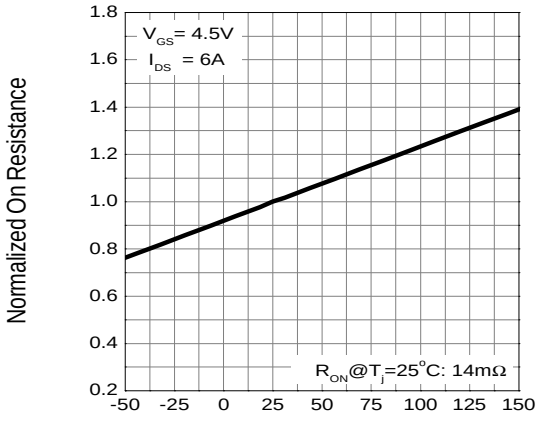
V_{GS} - Gate - Source Voltage (V)

Gate Threshold Voltage



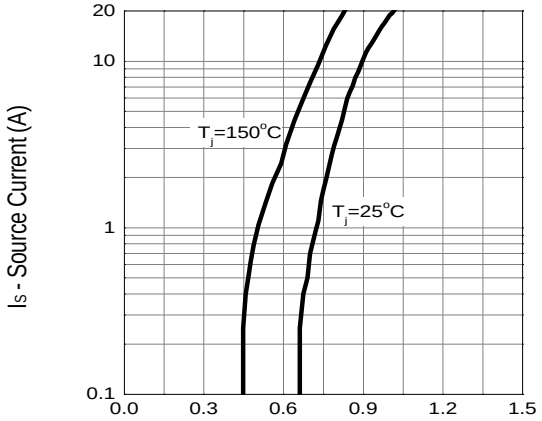
T_j - Junction Temperature (°C)

Drain-Source On Resistance



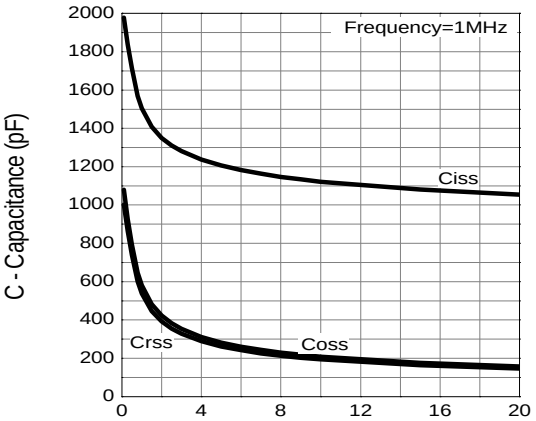
T_j - Junction Temperature (°C)

Source-Drain Diode Forward



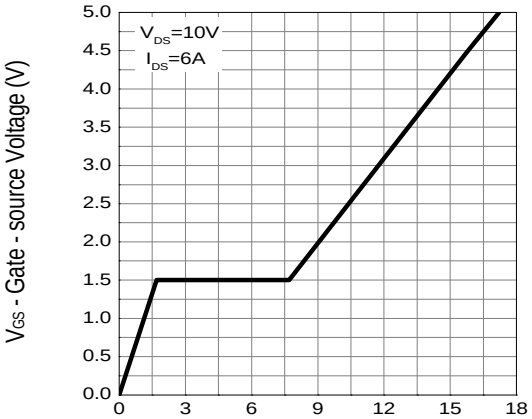
V_{SD} - Source - Drain Voltage (V)

Capacitance



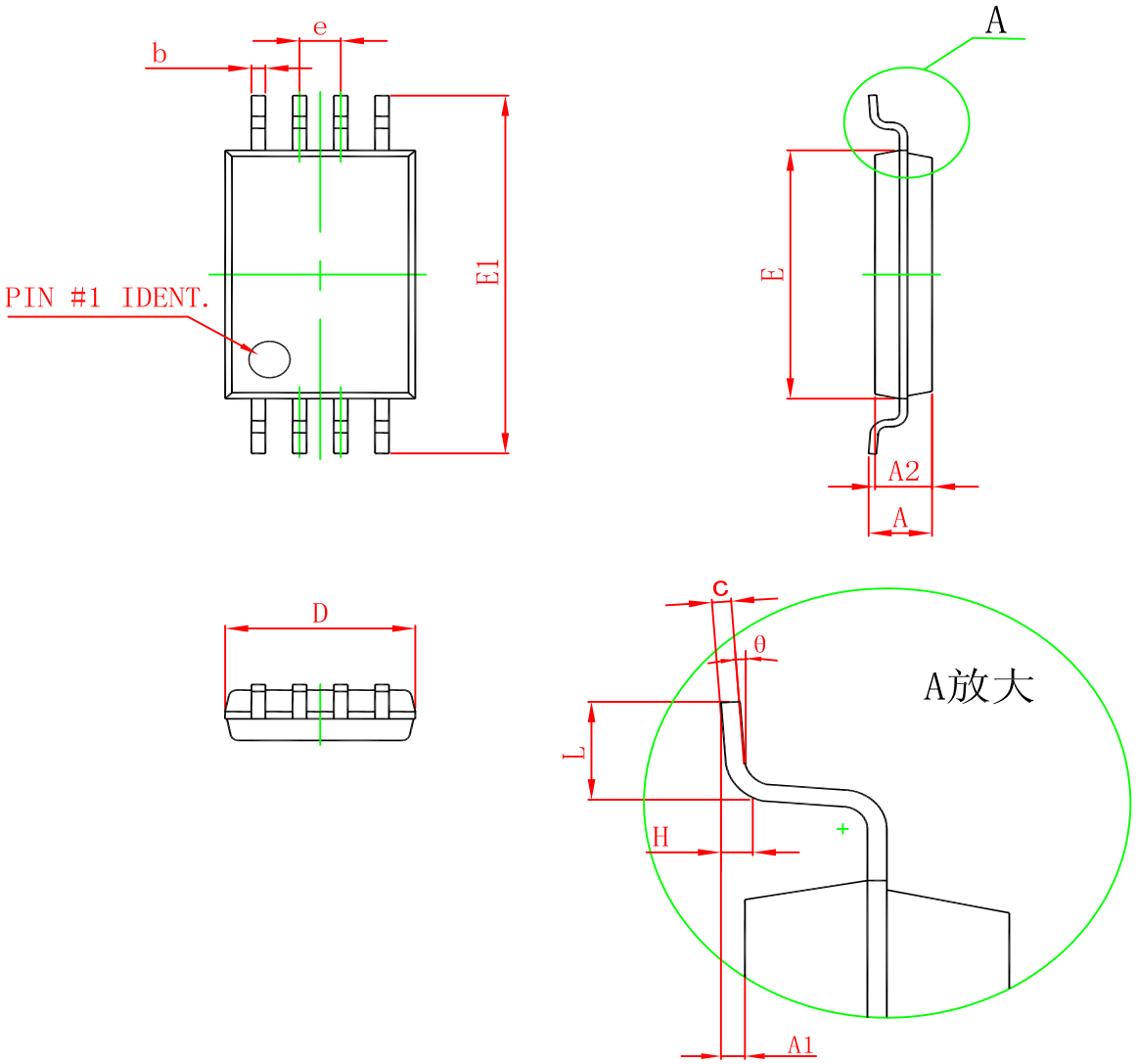
V_{DS} - Drain - Source Voltage (V)

Gate Charge



Q_G - Gate Charge (nC)

■ *TSSOP8L PACKAGE OUTLINE DIMENSIONS*

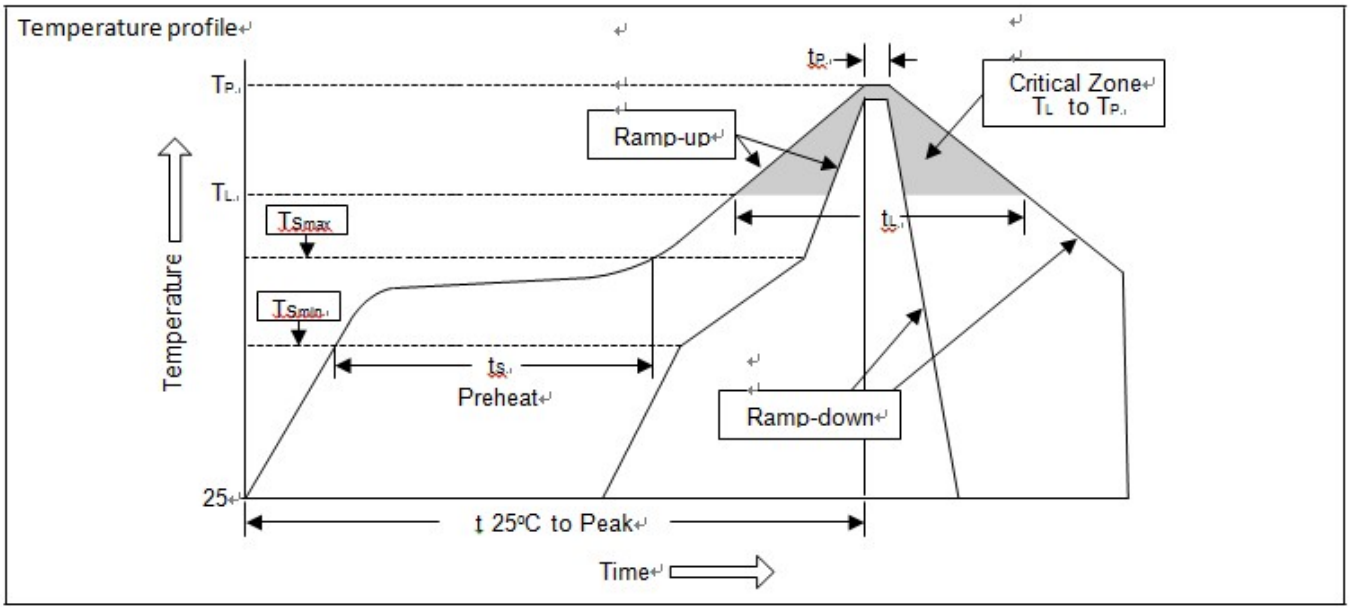


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.